SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

A HIGH EFFICIENCY, MIXED-TECHNOLOGY MOTOR DRIVER

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A new mixed technology called Multipower-BCD allows the integration of bipolar linear circuits, CMOS logic and DMOS power transistors on the same chip. This note describes a H-bridge motor driver IC realized with this technology.

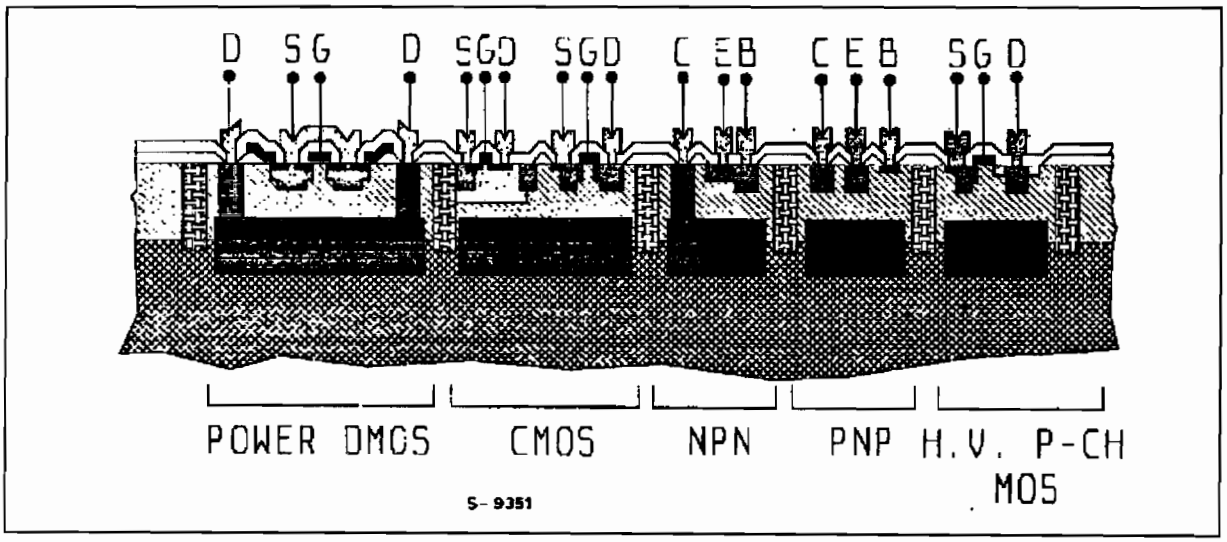
The miniaturization and integration of complex systems and subsystems has led in recent years to the implementation of monolithic circuits integrating logic functions and power sections.

For these applications SGS–THOMSON Microelectronics has developed a new technology called Multipower BCD which allows the integration on the same chip of isolated Power DMOS elements, bipolar transistors and C-MOS logic.

Thanks to high efficiency, fast switching speed and the absence of secondary breakdown, this technology is particularly suitable for fast, high current solenoid drivers and high frequency switching motor control. The free-wheeling diode intrinsic to the DMOS structure (necessary if the device drives an inductive load) and the great flexibility available in the choice of the logic and driving section components allow the complete integration of power actuators without further expense in silicon area-and a compact implementation of complex signal functions.

This technology has been applied to produce a switching power driver - the L6202/3 - capable of delivering 4A per phase, which is suitable for speed and position control in D.C. motor applications.

Figure 1 : A Schematic Cross Section of Bipolar, C-MOS, DMOS Structures (BCD).



MULTIPOWER BCD TECHNOLOGY

Multipower BCD technology combines the well known vertical DMOS silicon gate process, used for discrete POWER MOS devices, and the standard junction isolation, sinker and buried layer process. The architecture of the process is centred around the vertical DMOS silicon gate, a self aligned structure, which guarantees short channel length (1.5 μm) with consequent low $R_{DS(ON)}$ for the device.

In standard IC technologies the voltage capability is determined essentially by the thickness of the epitaxial layer and it is the same for signal and power components. But if the epi thickness is increased to allow the inclusion of high voltage transistors even the linear dimension of small signal transistors must be increased proportionally. In contrast MULTIPOWER BCD permits the realization of high voltage lateral DMOS structures in an epi-layer dimensioned for low voltage bipolar linear elements. Thus

it is possible to mix on the same die very dense CMOS logic, high precision bipolar linear circuits, very efficient DMOS power devices and high voltage lateral DMOS structures.

In this way the constraints which limit the complexity of signal processing circuits that can be integrated economically on a high chip are greatly reduced.

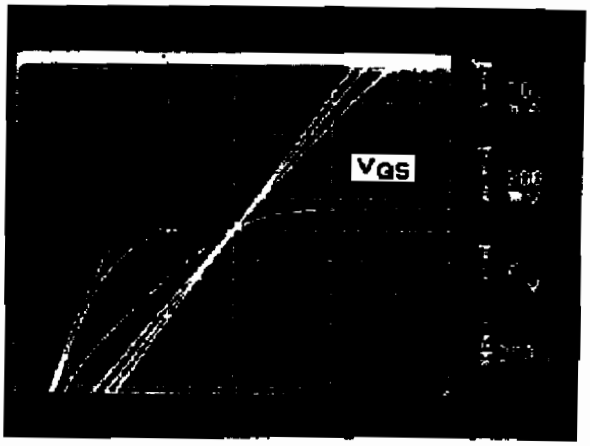
The active structures available in Multipower BCD technology are represented in fig. 1.

Within the vertical DMOS is indicated an intrinsic diode that can operate as a fast free-wheeling diode in switch mode applications. In fact DMOS, as a result of the way by which it is realized, is almost a symmetrical bidirectional device. That is, it can operate with the electrical I-V characteristic shown in the 3rd quadrant of fig. 2 ; that is, as a controlled resistor of value decreasing inversely with the gate source voltage applied to the power to which it is associated, up to a minimum equal to the $R_{DS(ON)}$ of the device itself, shunted by the body-drain diode intrinsic to the structure that limits the negative excursion of V_{DS}. Of the devices represented in fig. 1 the table 1 lists the electrical characteristics.

Table 1 : Devices in Multipower BCD Technology.

– Vertical DMOS	BV_{DSS} > 60V	$V_{TH} \cong 3V$	f_T > 1GHz
– Lateral DMOS	BV_{DSS} > 100V	$V_{TH} \cong 3V$	f_T > 800MHz
– P-channel with Drain Extension	BV_{DSS} > 85V	$V_{TH} \cong 3V$	f_T > 200MHz
– Bipolar NPN	LV_{CEO} > 20V	$\beta = 35$	f_T > 300MHz
– Bipolar PNP	LV_{CEO} > 20V	$\beta = 35$	f_T > 7MHz
– C-MOS N and P-channel	BV_{DSS} > 20V	$V_{TH} \cong 3V$	

Figure 2 : I-V Characteristic of DMOS N-channel Power Device.



THE L6202 & L6203 H-BRIDGE DRIVERS

Using this technology a H-bridge IC has been realized which accepts TTL or C-MOS compatible signals and is suitable for high efficiency, high frequency switching control of DC and stepping motor. The power stage consists of four DMOS N-channel transistors with $R_{DS(ON)} \equiv 0.3\ \Omega$.

When this device is supplied with the maximum voltage of 60V it can deliver a DC current of 1.5A in a standard DIP.16 (L6202) and up to 5A in a MULTIWATT package (L6203).

The device can also operate with a peak current of 8A for a time interval essentially determined by the time constant of heat propagation (< 200ms).

The system diagram representing the internal function blocks and external components (outside the dashed line) is shown in fig. 3.

The integrated circuit has 3 Inputs : Enable, Input 1, Input 2. When Enable is "low" all power devices are off ; when it is "high" their conduction state is controlled by the logic signals Input 1 and Input 2 that drive independently a single branch of the full bridge. When Input 1 (Input 2) is "high" DMOS 1 (DMOS 1') is "on" and DMOS 2 (DMOS 2') is "off", when is "low" DMOS 1 (DMOS 1') is "off" and DMOS 2 (DMOS 2') is "on".

A thermal protection circuit has been included that will disable the device if the junction temperature reaches 150 °C. When the thermal protection is removed the device restarts under the control of the Input and Enable signals.

ON-OFF SYNCHRONIZATION CIRCUIT

ON-OFF synchronization of the power devices located on the same leg of the bridge must prevent simultaneous conduction, with obvious advantages in terms of power dissipation and of spurious signals on the ground and on sensing resistors.

Because of the very short turn-on, turn-off times characteristic of POWER MOS devices a dead time (time in which all power transistors are "off") of 40 ns is sufficient to prevent rail-to-rail shorts. The circuit that provides this time interval is shown in fig. 4 with the voltage waveforms that explain how it works. Let us suppose Enable = "high". Because of the delay times introduced by INV1 and INV2, V2 and V3 are two waveforms contained one in the

Figure 3 : L6202-6203 Block Diagram.

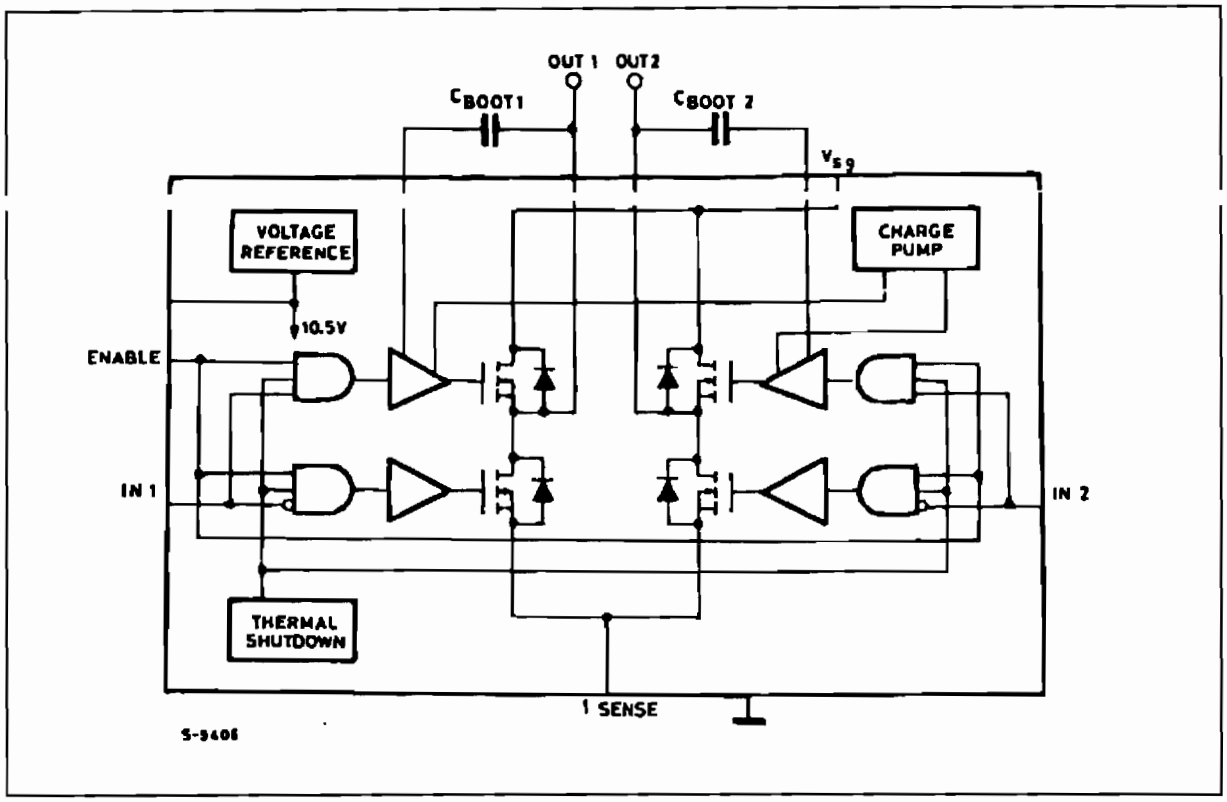
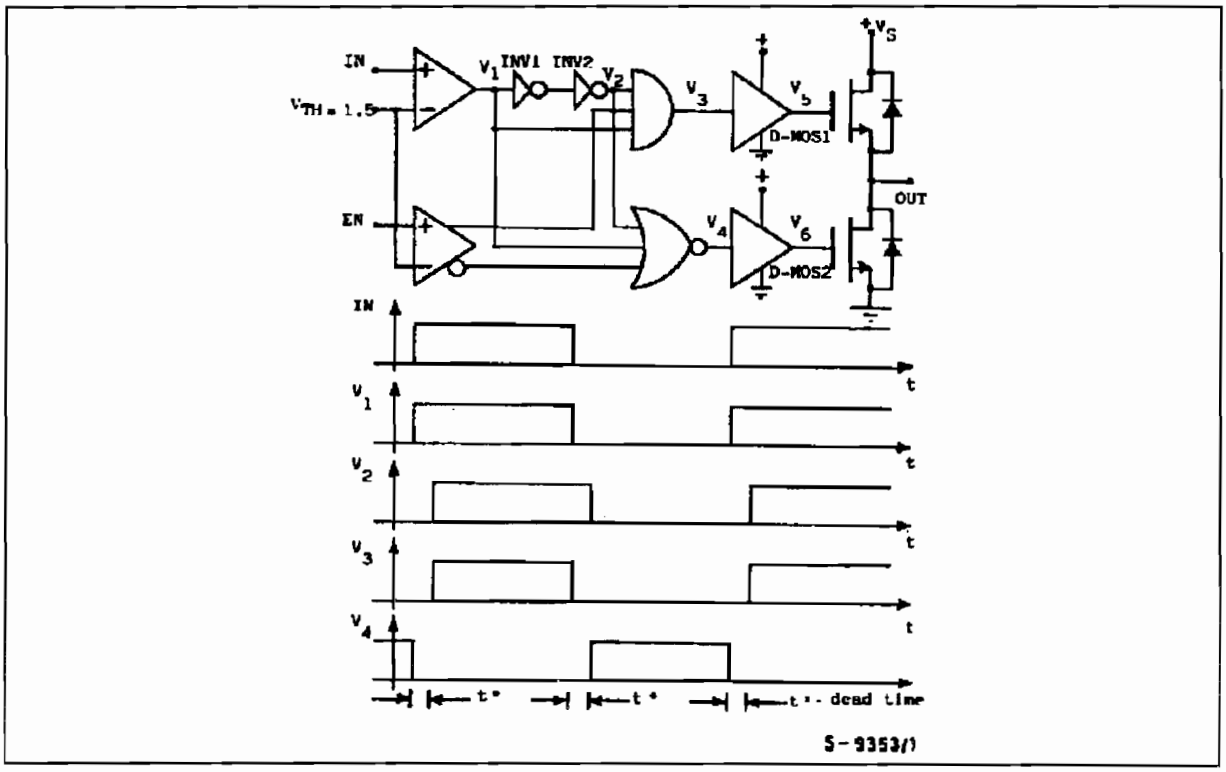


Figure 4 : A Schematic Representation of ON-OFF Synchronism Circuit.

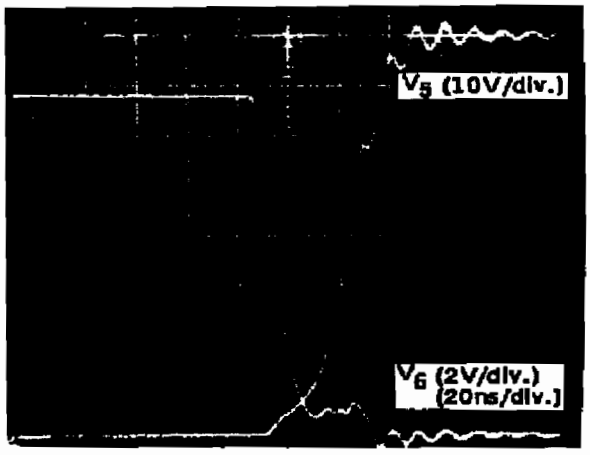


other and of polarity suitable to assure that the turn-on of a power transistor happens only after the turn-off of the other. The gate voltages V5 and V6 of DM1 and DM2 are represented in fig. 5. In fig. 3 we can see also the modality of operation of the Enable signal, charge pump and bootstrap circuits.

Concerning POWER MOS driving, it must be noted that it is necessary to assure to all DMOS N-channel a gate-source voltage of about 10V to guarantee full conduction of the POWER MOS itself. While there are no particular problems for driving the lower POWER MOS device (its terminals is referred to ground) for the upper one it is necessary to provide a gate voltage higher than the positive supply because it has the drain connected to the positive supply itself.

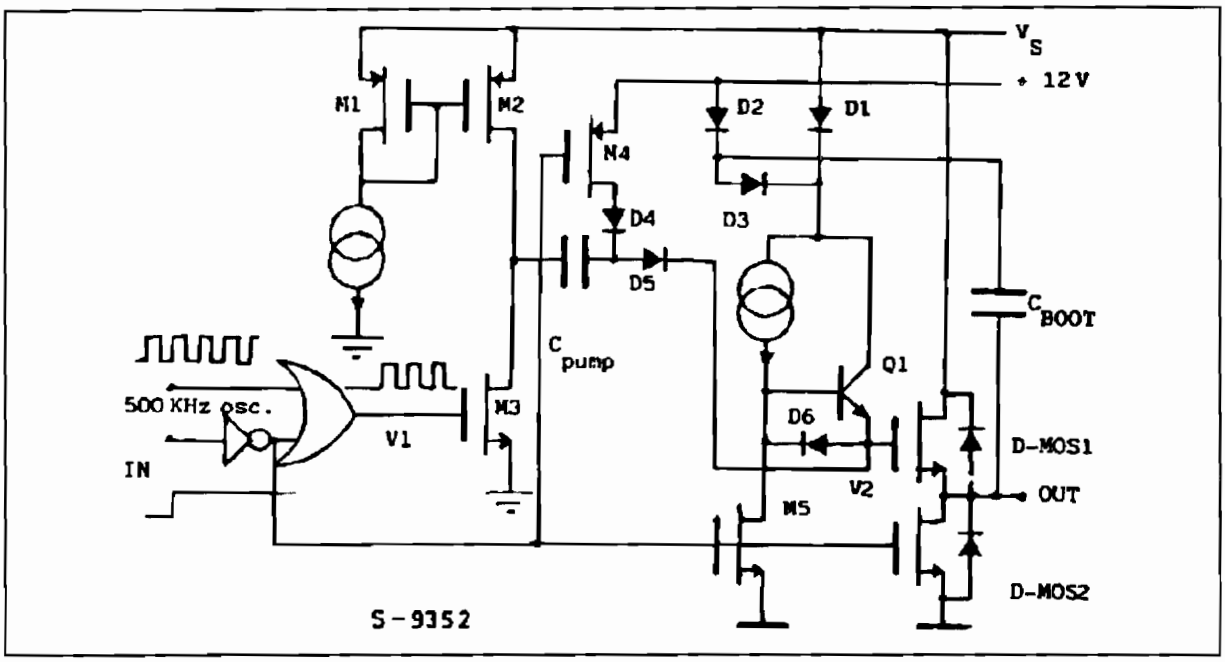
This is obtained using a system that combines a charge pump circuit, that assures DC operation, with a bootstrapping technique suitable to provide high switching frequencies. The circuit that satisfies to all these requirements is represented in the schematic diagram of fig. 6.

Figure 5 : POWER MOS Gate Voltage Waveforms.



In the description of this circuit we can assume that C_{BOOT} is absent and IN commutes from the "low" to the "high" level.

Figure 6 : Schematic Representation of Charge PUMP and BOOSTRAP Circuit used to Drive the Gate of the Upper DMOS Device.



In this condition, by means of D1, the circuit charges immediately the DMOS1 gate capacitance to V_S while the charge pump, activated by the signals IN = "low", as it can be seen in fig. 7, must supply only a voltage of about 10V.

In the switching operation it will be C_{BOOT} that guarantees a faster turn-on of the upper POWER MOS and consequently high commutation frequencies.

In fact during the period in which DMOS2 is "on" C_{BOOT} is charged to a voltage of about 12V.

When V_{out} raises because DMOS2 is disactivated D2 and D1 became "off" while D3, that remains "on"

connects the gate circuit to C_{BOOT} that raises higher than V_S and makes DMOS1 full "on" in a very short time interval (20 ns).

It must be noted that the switch M4 in the fig. 6 circuit, driven by a complementary phase respect to M3 disconnects D4, D5 and D6 from 12 V when M5 goes "on" to assure the "turn-off" of DMOS1.

Figure 7 : Charge PUMP Abilitation Signal and Gate Voltage of DMOS Upper Device.

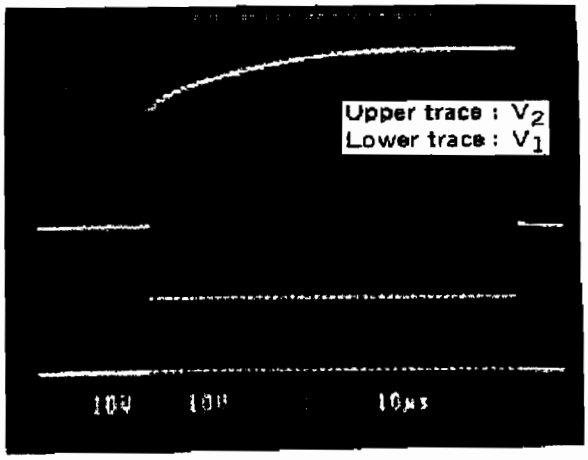
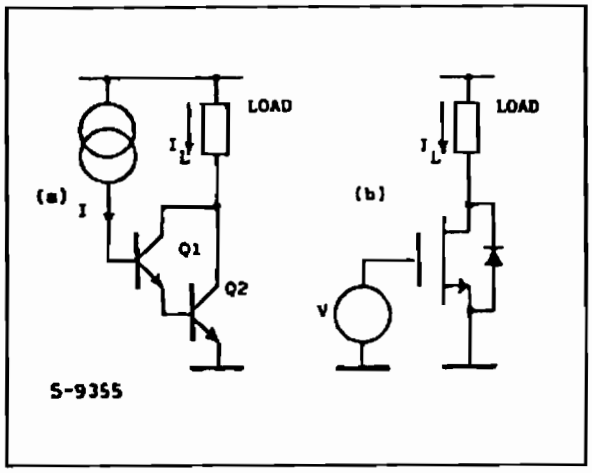


Figure 8 : Darlington Bipolar and DMOS Power Stages.



PERFORMANCE

One of the most important features is the very high efficiency achieved.

To appreciate the benefits of low power dissipation, and consequently of high efficiency, of a circuit realized in DMOS technology we must refer to the equivalent bipolar solution and also consider separate DC and AC operation.

Consider the typical Darlington power stage frequently used in integrated circuit and a DMOS power stages both represented in fig. 8.Neglecting the power dissipation in the driving section, in static conditions, the total dissipation of the two stages when they are "on" is in the case (a) :

$$P_{d(a)} = (V_{CESAT1} + V_{BE2}) \times I_L$$

and in the case (b) :

$$P_{d(b)} = R_{DS(ON)} \times I_L^2$$

where I_L is the load current.

Because the saturation loss of a power DMOS transistor can be reduced by increasing the silicon area it is possible to satisfy the condition

$$R_{DS\text{-}ON} \times I_L < (V_{CESAT1} + V_{BE2})$$

and then to obtain lower dissipation.

Concerning to the driving section, an other essential difference must be emphaisised.

While in case (a) during the time in which the power is "ON" it is necessary to supply a current for maintaining Q1 saturated, in the case (b) power is dissipated only during the commutation of the gate voltage.

About AC operation, it must be noted that the greatest advantage, always in terms of power dissipation, is due to the inherently fast turn-on, turn-offtimes of power MOS devices. In fact, if we suppose that the load is of inductive type and that the current waveform is triangular on the voltage commutation of the output, the total power dissipation is :

$$P_d = V_S \, I_L \, T_{COM.} \, f_{SWITCH}$$

where : V_S = Supply voltage, I_L = Peak load current,
$T_{COM.} = T_{TURN\text{-}ON} = T_{TURN\text{-}OFF}$,
f_{SWITCH} = Chopper frequency.

Because $T_{COM.}$ in DMOS case is ≤ than in bipolar case at a fixed frequency we have a lower dissipation or at fixed dissipation we can tolerate higher switching frequency.

Considering all these aspects, with a power device consisting of about 2200 cells we have realized DMOS power devices characterized by $R_{DS(ON)}$ 0.3 Ω and by switching times t_r, t_f of 50 ns. Other characteristics of the device when is configured as shown in fig. 9 are listed in table 2.

Fig. 10 shows the supply current with no load, vs. switching frequency.

Figure 9.

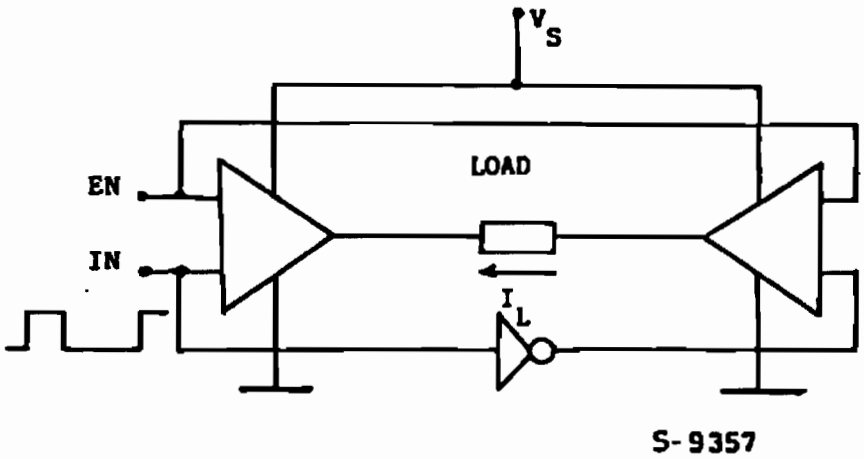


Table 2 : Main Features of L6202/6203.

V_S Maximum supply voltage	60V
I_L Maximum output current	1.5A (DIP16) 5A (MULTIWATT)
η Efficiency	90% (I_L = 1.5A; $f_{chopper}$ = 50kHz; V_S = 54V)
P_{tot} Power dissipation	1.5W
t_d turn-on, turn-off propagation delay	100ns

Figure 10.